APPARATUS AND METHOD FOR SELECTIVELY CONFIGURING A MEMORY DEVICE USING A BI-STABLE RELAY

ABSTRACT OF THE DISCLOSURE

The disclosed embodiments of the present invention include a semiconductor memory apparatus having a selectable memory capacity. In one embodiment, a system includes input, output, and data storage devices, a processor coupled to the devices, a memory device coupled to the processor, and a configuration circuit interposed between the processor and the memory device to selectively couple lines in the address, control and data busses of the processor to lines in the address, control and data busses of the memory device. In another embodiment, a memory device includes an array coupleable to one or more busses of an external device and a configuration circuit between the array and the busses of the external device to selectively couple the busses to the memory cell array. In a particular embodiment, the configuration circuit includes one or more bi-stable relays, such as Micro-Electrical-Mechanical System (MEMS) relays.